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EXAMINER	
CHERY, MARDOCHEE	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/039,010	OLARIG ET AL.	
	Examiner	Art Unit	
	Mardochee Chery	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

11-26-07

1)☒ Responsive to communication(s) filed on 10/25/07

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-6,8-11,13,16-18,20-27,29 and 32-48 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-6,8-11,13,16-18,20-27,29,32-48 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on October 25, 2007 has been entered.

Response to Amendment

2. In response to the last Office Action, independent claims 9, 32, and 36 are amended. Claims 47-48 are added. Claims 1-6, 8-11, 13, 16-18, 20-27, 29, 32-48 are now pending.

Response to Arguments

3. Applicant's arguments filed October 25, 2007 have been fully considered but they are not persuasive.

a. Applicant's representative argues on page 16, paragraph 2 of the remarks that Guttag does not disclose "a plurality of target devices with a single base address, wherein the same single base address is associated with each of the plurality of target devices" recited in claims 1, 9, 16, and 25.

Examiner strongly disagrees. Guttag incontestably discloses in haec verbae "each of a plurality of n processors has a predetermined plurality of corresponding memories, wherein the predetermined plurality of memories corresponding to each processor having a corresponding fixed base address;" and a base address instruction executing on any one of the plurality of n processors generating the base address of the predetermined plurality of memories corresponding to the one processor; col. 172, ll 48-60". Furthermore, it is abundantly clear in col. 5, lines 36-41 that Guttag discloses "a plurality of corresponding memories having a unique addressable memory of a single memory space wherein these corresponding memories have a corresponding base address within the single memory address space".

Applicant's representative further asserts that Guttag teaches that "each memory has its own unique base address". However, it is worth mentioning that Guttag discloses a one to one corresponce between the "plurality of memories" and the "**a** corresponding fixed base address" in contrast to applicant's representative assertion.

Leung also discloses associating the plurality of target devices with a single base memory address [col.4, lines 31-34]; and executing a memory access using the single base memory address [col.4, lines 44-46]. Furthermore, Leung discloses the "single base memory" address claimed by Applicant [col.4,

lines 30-35] where the base address can be associated with either a single target device or a group of target devices.

b. Applicant's representative argues on page 21 of the remarks that Gupta does not disclose "a plurality of devices simultaneously accessing associated interleaved memory regions in response to a single transaction" recited in claim 32.

Examiner strongly disagrees. Gupta discloses each of the devices simultaneously accesses its associated interleaved memory region in response to a single transaction requests [*two or more memory busses can each perform memory transactions simultaneously, with each memory bus coupled to one or more memory bus segments, wherein a single memory transaction can be active on a single memory bus segment at any given time, and each memory bus segment is coupled to one or more interleaved memory banks*; col. 16, ll 15-23].

Blaner still further discloses each of the devices simultaneously accesses its associated interleaved memory region in response to a single transaction requests [*interleaved memory banks wherein a group of the interleaved memory banks are accessible in parallel in response to a single access*; col. 8, ll 22-26].

c. Applicant's representative further asserts that there is nothing in Gupta with respect to the "plurality of devices having a common base address and simultaneous access of the plurality of devices to associated interleaved memory

region in response to a single transaction request directed to the common base address", recited in claim 32.

Examiner would like to point out that the newly added limitation to claim 32 is analogous to the limitation of "a plurality of target devices with a single base address, wherein the same single base address is associated with each of the plurality of target devices" in independent claims 1, 9, 16, and 25. As shown above, Guttag incontestably discloses in haec verbae "each of a plurality of n processors has a predetermined plurality of corresponding memories, wherein the predetermined plurality of memories corresponding to each processor having a corresponding fixed base address; and a base address instruction executing on any one of the plurality of n processors generating the base address of the predetermined plurality of memories corresponding to the one processor; col. 172, ll 48-60". Furthermore, it is abundantly clear in col. 5, lines 36-41 that Guttag discloses "a plurality of corresponding memories having a unique addressable memory of a single memory space wherein these corresponding memories have a corresponding base address within the single memory address space". It is worth mentioning that Guttag discloses a one to one corresponce between the "plurality of memories" and the "**a** corresponding fixed base address" in contrast to applicant's representative assertion.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. Claims 32 and 47-48 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. In particular, claim 32 recites inter alias a plurality of devices "having a common base address" and a single transaction request "directed to the common base address". Claims 47 recites inter alias "assigning a common base address to a plurality of disk drives to create a collective target group; initiating an interleaved memory operation...using the common base address, wherein each disk drive recognizes the common base address and simultaneously executes the memory operation on the portion of data storage to which the disk drive is assigned". Although the original disclosure provides for "a single base address", it does not provide for these newly added limitations. As such, claims 32 and 47-48 are rejected under 35 USC 112 first paragraph for containing new matter.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1-6, 8-11, 13, 16-18, 20-23, 25-27 and 29 are rejected under 35 U.S.C 103(a) as being unpatentable over Leung et al. (US 6,272,577) in view of Guttag (5,761,726).

As per claim 1, Leung et al. discloses a method for transacting between an initiator device and a plurality of target devices [*a memory device in which a single input data stream can be simultaneously written to multiple memory arrays*; col.3, lines 63-65]; sending a multicast transaction from the initiator device to the plurality of target devices, wherein sending the multicast transaction comprises sending a multicast transaction to the single base address associated with each of the plurality of target devices [*a base address which identifies the memory module*; col.10, lines 20-23; *the memory modules are equipped with independent address and command decoders so that they function as independent units, each with their own base address*; *the present invention groups at least two memory arrays or banks into a memory module and connects all the memory modules to a bus*; col.4, lines 20-24; *in each memory module, a programmable identification register contains the base address of the memory module and a mechanism which decommissions the module from acting on certain memory access*; col.5, lines 5-8; col.4,

lines 31-33; *multiple bank operations such as broadcast-write and interleaved access possible; a memory device able to handle a broadcast write operations simultaneously*; col.5, lines 27-31]; executing the transaction when the transaction is received by the plurality of target devices according to the configuration of the target devices [*since each memory module is a complete functional unit, the memory module architectures allows parallel processes and multiple memory module operations to be performed within different memory modules*; col.4, lines 42-45].

However, Leung does not explicitly teach associating each of the plurality of target devices with a single base address, wherein the same single base address is associated with each of the plurality of target devices as recited in the claim.

Guttag discloses associating each of the plurality of target devices with a single base address, wherein the same single base address is associated with each of the plurality of target devices [col.172, lines 48-55] to generate addresses for read/write access to data stored within a plurality of memories (col. 5, ll 40-45).

Since the technology for implementing a data processing system with associating each of the plurality of target devices with a single base address, wherein the same single base address is associated with each of the plurality of target devices was well known as evidenced by Guttag, an artisan would have been motivated to implement this feature in the system of Leung in order to generate addresses for read/write access to data stored within a plurality of memories. Thus, it would have been obvious to one of ordinary skill in the art at the time of invention by Applicant to modify the system of Leung to include associating each of the plurality of target devices with a single base

address, wherein the same single base address is associated with each of the plurality of target devices because this would have generated addresses for read/write access to data stored within a plurality of memories (col. 5, ll 40-45) as taught by Guttag.

As per claim 2, Leung et al. discloses assigning a base memory address to be shared by the plurality of target devices [*a base address which identifies the memory module*; col.10, lines 20-23; *a memory device in which a single input data stream can be simultaneously written to multiple memory arrays*; col.3, lines 63-65]; and assigning a first portion of memory to a first target device of the plurality of target devices [*each memory module has independent address and command decoders to enable independent operation so that each memory module is activated only when a memory access operation is performed*; abstract].

As per claim 3, Leung et al. discloses the transaction is a read request for a block of stored data from memory [*a read or write command causes data to be read or written to different arrays in a time multiplexed data burst*; col.24, lines 23-27; *the address information comprises a base address of the memory device to be accessed*; col.31, lines 12-14]; recognizing the base memory address from the read request *[each memory module has independent address and command decoders to enable independent operation so that each memory module is activated only when a memory access operation is performed*; abstract ; *the memory modules are equipped with independent address and command decoders so that they function as independent units, each with their own base address*; col.4, lines 31-33]; initiating a read operation by the plurality of target devices assigned to the base memory address [*each memory module has independent address and command decoders to enable independent operation so that each memory module is activated only*

when a memory access operation is performed; abstract; *a read or write command causes data to be read or written to different arrays in a time multiplexed data burst*; col.24, lines 23-27; *a base address which identifies the memory module*; col.10, lines 20-23]; fetching stored data from a portion of memory associated with each of the target devices, the data being concurrently fetched by each associated target device and sending the fetched data to the initiator device [*another multiple-array operation is an interleaved burst operation, in which a read or write command causes data to be read or written to different arrays in a time multiplexed data burst*; col.24, lines 23-27].

As per claim 4, Leung et al. discloses, the transaction is a write request for data to be stored in memory [*a read or write command causes data to be read or written to different arrays in a time multiplexed data burst*; col.24, lines 23-27]; recognizing the base memory address from the write request [*address information comprises a base address of the memory device to be accessed*; col.31, lines 13-14; *a read or write command causes data to be read or written to different arrays in a time multiplexed data burst*; col.24, lines 23-27]; initiating a write operation by the plurality of target devices assigned to the base memory address [*each memory module has independent address and command decoders to enable independent operation so that each memory module is activated only when a memory access operation is performed*; abstract; *a base address which identifies the memory module*; col.10, lines 20-23]; and writing data of the write request to a portion of memory associated with each target device, the data being concurrently written by each associated target device[*another multiple-array operation is an interleaved burst operation, in which a read or write command causes data to be read or written to different arrays in a time multiplexed data burst*; col.24, lines 23-27].

As per claim 5, Leung et al. discloses, wherein the target devices comprise input/output Controllers [*I/O module 104 contains a controller*; col.7, lines 46-47].

As per claim 6, Leung et al. discloses, the target devices comprise disk array controllers [Fig. 19; *controller 1920*].

As per claim 8, Leung et al. discloses, a plurality of target groups [*the present invention groups at least two memory arrays or banks into a memory module and connects all the memory modules to a bus*; col.4, lines 20-24].

As per claim 9, the rationale in the rejection of claim 1 is herein incorporated. Leung et al. further discloses, a method for transacting data stored in memory between an initiator device and detecting a multicast transaction request [*multiple bank operations such as broadcast-write and interleaved access possible; a memory device able to handle a broadcast write bandwidth of 36 gigabytes per second and 36 memory operations simultaneously*; col.5, lines 27-31]; accessing a first portion of memory by a first target device associated with the first portion of memory in response to the multicast transaction request [*when a memory read or write command is decoded, each memory module examines the communication ID of the command. All modules, except the module to which the command is addressed, go into an idle state until the read or write transaction is finished*; col.19, lines 42-47]; accessing a second portion of memory by a second target device associated with the second portion of memory concurrently with access to the first portion of memory in response to the multicast transaction request

wherein the first and second portions of memory are accessed with a single base address associated with the first target device and the second target device [*a first field contains a base address which identifies the memory module by communication address. A second field contains an address which identifies the memory array within the memory module*. col.10, lines 21-25; *the present invention groups at least two memory arrays or banks into a memory module and connects all the memory modules to a bus*; col.4, lines 20-24; *in each memory module, a programmable identification register contains the base address of the memory module and a mechanism which decommissions the module from acting on certain memory access*; col.5, lines 5-8;].

As per claim 10, Leung et al. discloses, the target devices comprise input/output Controllers [*I/O module 104 contains a controller*; col.7, lines 46-47].

As per claim 11, Leung et al. discloses, the target devices comprise disk array Controllers [Fig. 19; *controller 1920*].

As per claim 13, Leung et al. discloses accessing a plurality of target devices, wherein the plurality of target devices are divided into a plurality of groups, wherein each of the plurality of groups is associated with a single base memory address configured to address the target devices within that group [*the present invention groups at least two memory arrays or banks into a memory module and connects all the memory modules to a bus*; col.4, lines 20-24; *in each memory module, a programmable identification register contains the base address of the memory module and a mechanism which decommissions the module from acting on certain memory access*; col.5, lines 5-8].

As per claim 16, the rationale in the rejection of claim 1 is herein incorporated. Leung et al. further discloses, a computer system comprising a bus [*memory device and allowing each memory module to have a communication address on the I/O bus system*; col.4, lines 54-56]; an initiator device coupled to the communications bus for initiating a transaction request [*all memory transactions are initiated by either I/O module 104 or by devices connected to I/O bus 106*; col.7, lines 45-46]; and a plurality of target devices coupled to the communications for executing the transaction request, the plurality of target devices executing the transaction request by each target device concurrently responding to a portion of the transaction request, wherein the initiator device is configured to multicast a transaction request to the plurality of target devices using a single base address associated with the plurality of target devices [*a first field contains a base address which identifies the memory module by communication address. A second field contains an address which identifies the memory array within the memory module*. col.10, lines 21-25; *a memory device in which a single input data stream can be simultaneously written to multiple memory arrays*; col.3, lines 63-65; *a memory device in accordance with the present invention provides multiple commands, one after another, to different arrays*; col.25, lines 15-17; *a base address which identifies the memory module*; col.10, lines 20-23; *the memory modules are equipped with independent address and command decoders so that they function as independent units, each with their own base address*; *the present invention groups at least two memory arrays or banks into a memory module and connects all the memory modules to a bus*; col.4, lines 20-24].

As per claim 17, Leung et al. discloses the target device comprises input/output controllers [*I/O module 104 contains a controller*; col.7, lines 46-47].

As per claim 18, Leung et al. discloses a target device comprises disk array controllers [Fig. 19; *controller 1920*].

As per claim 20, Leung et al. discloses the plurality of target devices comprise a target group [*the present invention groups at least two memory arrays or banks into a memory module and connects all the memory modules to a bus*; col.4, lines 20-24].

As per claim 21, Leung et al. discloses a plurality of target groups [*the present invention groups at least two memory arrays or banks into a memory module and connects all the memory modules to a bus*; col.4, lines 20-24].

As per claim 22, Leung et al. discloses the transaction is a multicast read request [*all memory transactions are initiated by either I/O module 104 or by devices connected to I/O bus 106*; col.7, lines 45-46; *when a memory read or write command is decoded, each memory module examines the communication ID of the command*; col.19, lines 42-47].

As per claim 23, Leung et al. discloses the transaction is a multicast write request [*multiple bank operations such as broadcast-write and interleaved-access*; col.5, lines 27-29; *a memory device in which a single input data stream can be simultaneously written to multiple memory arrays*; col.3, lines 63-65].

As per claim 25, the rationale in the rejection of claim 1 is herein incorporated. Leung et al. further discloses a computer system comprising a processor, a bus coupled to the processor [*the two processors can reside on the same bus using the same memory module*; col.10, lines 40-42]; an initiator device coupled to the bus for issuing a multicast transaction, and a plurality of target devices coupled to the bus for executing the multicast transaction with concurrent data responses from a plurality of interleaved memory regions, wherein the initiator device is configured to multicast the transaction request to the plurality of target devices using a single base address associated with the plurality of target devices [*all memory transactions are initiated by either I/O module 104 or by devices connected to I/O bus 106*; col.7, lines 45-46; *multiple bank operations such as broadcast-write and interleaved access possible. A memory device able to handle a broadcast write bandwidth of 36 gigabytes per second and 36 memory operations simultaneously*; col.5, lines 27-31; *a first field contains a base address which identifies the memory module by communication address;* col.10, lines 21-25; *the present invention groups at least two memory arrays or banks into a memory module and connects all the memory modules to a bus*; col.4, lines 20-24; *in each memory module, a programmable identification register contains the base address of the memory module and a mechanism which decommissions the module from acting on certain memory access*; col.5, lines 5-8].

As per claim 26, Leung et al. discloses the target devices comprise input/output controllers [*I/O module 104 contains a controller*; col.7, lines 46-47].

As per claim 27, Leung et al. discloses the target devices comprise disk array

Controllers [Fig. 19].

As per claim 29, Leung et al. discloses a plurality of target devices are divided into a plurality of target groups, wherein each of the target groups is associated with its own base address [*the present invention groups at least two memory arrays or banks into a memory module and connects all the memory modules to a bus*; col.4, lines 20-24; *in each memory module, a programmable identification register contains the base address of the memory module and a mechanism which decommissions the module from acting on certain memory access*; col.5, lines 5-8].

8. Claim 24 is rejected under 35 U.S.C. 103(a) as being unpatentable over Leung in view of Guttag (5,761,726) and further in view of Carmichael et al. (US 5,864,712).

As per claim 24, Leung and Guttag disclose the claimed invention as detailed above in the previous paragraphs. However, Leung and Guttag do not explicitly teach the communications bus comprises a Peripheral Component Interconnect (PCI) bus as recited in the claim.

Carmichael discloses the bus comprises a Peripheral Component Interconnect (PCI) bus [*the bridge 36 may simply provide an extension of the processor's bus, or may buffer and extend the processor bus using an entirely different bus structure and protocol such as PCI*; col.6, lines 46-50] to provide an extension of the processor's bus and to buffer and extend the processor (col.6, lines 46-50).

Since the technology for implementing a data processing system using a PCI bus was well known in the art as evidenced by Carmichael, and since a PCI bus provides an extension of the processor's bus and to buffer and extend the processor, an artisan would have been motivated to implement a PCI bus in the data processing system of Leung and Guttag. Thus it would have been obvious to one of ordinary skill in the art, at the time the invention was made, to modify the system of Leung and Guttag to include a PCI bus to provide an extension of the processor's bus and to buffer and extend the processor (col.6, lines 46-50) as taught by Carmichael.

9. Claims 32 and 47 are rejected under 35 U.S.C. 103(a) as being unpatentable over Guttag 5,761,726) Gupta (6,405,286) in view of Blaner (5,737,575).

As per claim 32, Guttag discloses a plurality of devices having a common base address and a transaction request directed to the common base address [*each of a plurality of n processors has a predetermined plurality of corresponding memories, wherein the predetermined plurality of memories corresponding to each processor having a corresponding fixed base address; and a base address instruction executing on any one of the plurality of n processors generating the base address of the predetermined plurality of memories corresponding to the one processor*; col. 172, ll 48-60; *a plurality of corresponding memories having a unique addressable memory of a single memory space wherein these corresponding memories have a corresponding base address within the single memory address space;* col. 5, lines 36-41]. It is worth mentioning that Guttag discloses a one to one corresponce between the "plurality of memories" and the "**a** corresponding fixed base address".

Gupta discloses a computer comprising a memory [col.1, lines 24-25]; a controller configured to logically divide the memory into a plurality of interleaved memory regions [Fig.2]; and a plurality of devices, wherein each of the plurality of devices is associated with one of the interleaved memory regions and wherein each of the devices simultaneously accesses its associated interleaved memory region in response to a single transaction request [col.6, lines 21-28; col. 16, ll 12-24] so that multiple CPUs tend not access the same memory bank at the same time (col. 6, lines 23-26].

Gupta further discloses each of the devices simultaneously accesses its associated interleaved memory region in response to a single transaction requests [*two or more memory busses can each perform memory transactions simultaneously, with each memory bus coupled to one or more memory bus segments, wherein a single memory transaction can be active on a single memory bus segment at any given time, and each memory bus segment is coupled to one or more interleaved memory banks*; col. 16, ll 15-23].

Blaner incontestably discloses each of the devices simultaneously accesses its associated interleaved memory region in response to a single transaction requests [*interleaved memory banks wherein a group of the interleaved memory banks are accessible in parallel in response to a single access*; col. 8, ll 22-26] to allow simultaneous access to multiple pages of memory and reduce latency (col. 2, ll 65-67).

Since the technology for implementing a memory system with devices each simultaneously accessing its associated interleaved memory region in response to a single transaction requests was well known as evidenced by Blaner, an artisan would have been motivated to implement this feature in the system of Gupta to allow

simultaneous access to multiple pages of memory and reduce latency. Thus, it would have been obvious to one of ordinary skill in the art at the time of invention by Applicant to modify the system of Gupta in view of Blaner to include devices each simultaneously accessing its associated interleaved memory region in response to a single transaction requests because this would have allowed simultaneous access to multiple pages of memory and reduced latency (col. 2, ll 65-67) as taught by Blaner.

As per claim 47, Guttag discloses a method of performing operations accessing memory comprising assigning a common base address to a plurality of disk drives to create a collective target group [col. 172, ll 48-60; col. 5, lines 36-41].

Gupta further discloses assigning a portion of data storage to each disk drive of the collective target group [Fig. 1] so that multiple CPUs tend not access the same memory bank at the same time (col. 6, lines 23-26].

Blaner discloses initiating an interleaved memory operation as a single request to the collective target group using the common base address, wherein each disk drive recognizes the common base address and simultaneously executes the memory operation on the portion of data storage to which the disk drive is assigned [*interleaved memory banks wherein a group of the interleaved memory banks are accessible in parallel in response to a single access*; col. 8, ll 22-26] to allow simultaneous access to multiple pages of memory and reduce latency (col. 2, ll 65-67).

10. Claim 48 is rejected under 35 U.S.C. 103(a) as being unpatentable over Guttag 5,761,726) Gupta (6,405,286) in view of Blaner (5,737,575) and further in view of Olarig (6,230,225).

As per claim 48, initiating an interleaved memory operation as a single request comprises initiating a multicast transaction from a SCUSI controller over a multicast bus [Fig.1, col. 1, lines 26-51] to broadcast a single bus transaction to multiple targets (col.1, lines 5-10).

11. Claims 33-38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Leung et al. (US 6,272,577) in view of Guttag (5,761,726) and further in view of Gupta (6,405,286).

As per claim 33, the rationale in the rejection of claim 1 is herein incorporated. However, Leung and Gutttag do not explicitly teach a method comprising dividing a section of memory into a plurality of interleaved memory regions as required by the claim.

Gupta discloses a method comprising dividing a section of memory into a plurality of interleaved memory regions [col.6, lines 20-24] so that multiple CPUs tend not to access the same memory bank at the same time (col.6, ll 23-26).

Since the technology for implementing a data processing system with dividing a section of memory into a plurality of interleaved memory regions was well known as evidenced by Gupta, an artisan would have been motivated to implement this feature in the system of Leung and Guttag] so that multiple CPUs would not tend to access the same memory bank at the same time. Thus, it would have been obvious to one of ordinary skill in the art at the time of invention by Applicant to modify the system of Leung Guttag to include dividing a section of memory into a plurality of interleaved memory regions because this would have allowed multiple CPUs not to tend accessing the same memory bank at the same time (col.6, ll 23-26) as taught by Gupta.

AS per claim 34, Gupta discloses executing the memory access comprises executing a read operation [col.6, lines 24-27].

As per claim 35, Gupta discloses executing the memory access comprises executing a write operation [col.6, lines 24-27].

As per claim 36, the rationale in the rejection of claim 1 is herein incorporated. Gupta further discloses a tangible machine readable medium comprising code to initialize a plurality of devices [col.11, lines 36-39]; and code to associate the single base address with a plurality of interleaved memory regions [col.6, lines 21-23]; col.12, lines 44-55].

As per claim 37, Gupta discloses code to issue a single read command comprising the single base address [col.6, lines 11-14; col.4, lines 31-34; col.6, lines 53-54]; code to recognize the single base address as associated with the plurality of devices [col.10, lines 20-23; col.6, lines 53-54]; code to simultaneously execute a plurality of memory requests involving the plurality of devices [col.6, lines 21-28; col.6, lines 53-54]; code to receive data from the plurality of devices [col.8, lines 11-12; col.6, lines 53-55]; and code to write the received data to a bus [col.8, lines 14-16].

As per claim 38, Gupta discloses code to issue a write command comprising the single base address [col.6, lines 12-15; col.4, lines 31-34; col.6, lines 53-56]; code to recognize the base address as associated with the plurality of devices [col.4, lines 31-34; col.6, lines 53-56]; and code to simultaneously write to the plurality of devices [col.6, lines 21-28].

12. Claims 39-44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Leung et al. (US 6,272,577) in view of Guttag (5,761,726) and further in view of Olarig (6,230,225).

As per claim 39, Olarig discloses the multicast transaction comprises sending the multicast transaction from a disk controller to a plurality of disk drives [Fig.1, *PCI device 150A, PCI Bridge 130, Memory 180*] to broadcast a single bus transaction to multiple targets (col.1, lines 5-10).

Since the technology for implementing a data processing with sending multicast transaction to a plurality of disk drives was well known as evidenced by Olarig, an artisan would have been motivated to implement this feature in the system of Leung and Guttag since this would have enabled broadcasting of a single bus transaction to multiple target devices. Thus, it would have been obvious to one of ordinary skill in the art at the time of invention by applicant, to modify the system of Leung and Guttag to include sending multicast transaction to a plurality of disk drives because this would have enabled broadcasting of a single bus transaction to multiple target devices (col.1, lines 5-10) as taught by Olarig.

As per claims 40-41, and 43-44, Olarig discloses sending the multicast transaction comprises sending the multicast transaction from a SCSI controller to a plurality of SCSI devices [Fig.1, col.1, lines 26-51].

As per claim 42, Olarig discloses the plurality of target devices comprises a plurality of disk drives [Fig.1, memory 180-190].

13. Claims 45-46 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gupta (US 6,405,286) in view of Blaner (5,737,575) and further in view of Olarig (6,230,225).

As per claims 45-46, Olarig discloses sending the multicast transaction comprises sending the multicast transaction from a SCSI controller to a plurality of SCSI devices [Fig.1, col.1, lines 26-51].

Conclusion

14. When responding to the office action, Applicant is advised to clearly point out the patentable novelty that he or she thinks the claims present in view of the state of the art disclosed by references cited or the objections made. He or she must also show how the amendments avoid such references or objections. See 37 C.F.R. 1.111(c).

15. When responding to the Office action, Applicant is advised to clearly point out where support, with reference to page, line numbers, and figures, is found for any amendment made to the claims.

16. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mardochee Chery whose telephone number is (571) 272-4246. The examiner can normally be reached on 8:30A-5:00P.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hyung Sough can be reached on (571) 272-6799. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

November 20, 2007

HYUNG S. SOUGH
SUPERVISORY PATENT EXAMINER
11/26/07

Mardochee Chery
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